ELECTRODE STRUCTURE FOR USE IN AN INTEGRATED CIRCUIT

Field of the Invention

The present invention relates generally to semiconductor chips and integrated circuits, and more particularly to an electrode structure for use in integrated circuits, such as electronic systems, memory systems and the like.

Background of the Invention

In fabricating integrated circuits, semiconductor chips and the like, chemical/mechanical planarization can be used as an intermediate operation to planarize a structure to provide a uniform, level surface for subsequent processing operations in the manufacturing of a semiconductor chip or integrated circuit. For example, electrodes or electrical contacts between different layers of conductive materials in a semiconductor chip can be formed by depositing a first layer of conductive material, typically a metal, although a semiconductor material could be used as well, and then depositing a thin dielectric layer over the first conductive layer. The dielectric layer is then patterned to form at least one opening in the dielectric layer to expose a portion of the surface of the first conductive layer. The opening can have a small aspect ratio of depth to width. For instance, the opening can be about half a micron wide but only about 500 angstroms deep thus presenting a aspect ratio of about 0.1. A second layer of a different conductive material is then deposited on the dielectric layer and in the opening on the first conductive layer to make electrical contact through the opening with the first conductive layer. The second conductive layer is then removed form the dielectric layer or planarized to expose the dielectric layer and to form an isolated electrode or damascene contact structure in the opening before subsequent fabrication operations. In removing the second conductive layer by chemical/mechanical processing or planarization (CMP), the forces created by the CMP process can have a tendency to force the conductive material of the second layer out of the opening thereby destroying the contact.

Accordingly, for the reason stated above, and for other reasons that will become apparent upon reading and understanding the present specification, there is a need for an electrode structure and method of fabrication that provides substantially improved adhesion between a first layer of conductive material and second layer of a different conductive material, particularly during a CMP operation, and that does not adversely effect the conductivity between the two layers or create an electrical barrier. There is also a need for a method of fabricating an electrode structure that does not effect or damage other components that may already have been formed on the same wafer or substrate and that does not adversely effect the manufacturing process by requiring a significant number of additional process operations.

Summary of the Invention

The above mentioned problems with electrode structures are addressed by the present invention and will be understood by reading and studying the following specification. Electrode structures, memory cells and systems are provided by the present invention that exhibit good adhesion between different conductive layers during manufacturing operations such as CMP without the conductivity between the layers being adversely effected. Methods of fabricating are also provided by the present invention that do not adversely effect other components that may have already been formed on a semiconductor die.

In accordance with the present invention, an electrode structure includes a first layer of conductive material and a dielectric layer formed on a surface of the first layer. An opening is formed in the dielectric layer to expose a portion of the surface of the first layer. A binding layer is formed on the dielectric layer and on the exposed portion of the surface of the first layer and a second layer of conductive material is formed on the conductive binding layer.

In accordance with an embodiment of the present invention, a memory cell, includes a first layer of conductive material and a dielectric layer formed on a surface of the first layer. An opening is formed in the dielectric layer to expose a

portion of the surface of the first layer. A binding layer is formed on the dielectric layer and on the exposed portion of the surface of the first layer and a second layer of conductive material is formed on the binding layer. A layer of doped chalcogenide material is formed on the second layer of conductive material and a third layer of conductive material is formed on the layer of doped chalcogenide material.

In accordance with another embodiment of the present invention, a method of making an electrode, comprises: forming a first layer of conductive material; forming a dielectric layer on a surface of the first layer; forming an opening in the dielectric layer to expose a portion of the surface of the first layer; forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer; and forming a second layer of conductive material on the binding layer. The electrode structure can be annealed at a selected temperature for a predetermined time period to cause conductive material from the second layer to be diffused into the binding layer to improve adhesion and conductivity between the first and second conductive layers.

In accordance with another embodiment of the present invention, a method of making a memory cell, comprises: forming a first layer of conductive material; forming a dielectric layer on a surface of the first layer; forming an opening in the dielectric layer to expose a portion of the surface of the first layer; forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer; forming a second layer of conductive material on the binding layer; forming a layer of doped chalcogenide material on the second layer of conductive material; and forming a third layer of conductive material on the layer of doped chalcogenide material. The layer of chalcogenide material can be doped by annealing the memory cell to cause conductive material from the third layer to be chemisorbed into the chalcogenide layer.

These and other embodiments, aspects, advantages and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following

description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

In the drawings, like numerals describe substantially similar components throughout the several views. Like numerals having different letter suffixes or primed (X') represent different occurrences of substantially similar components.

Figures 1A-1C illustrate the operations in forming an electrode for use in an integrated circuit in accordance with the present invention.

Figures 2A-D illustrate the operations in forming a programmable memory cell in accordance with an embodiment of the present invention.

Figures 3A-3E illustrate the operations in forming a programmable memory cell in accordance with another embodiment of the present invention.

Figure 4 is a schematic diagram of a memory system incorporating a programmable memory cell in accordance with the present invention.

Figure 5 is a top view of a wafer or substrate containing semiconductor dies in accordance with an embodiment of the present invention.

Figure 6 is a block schematic diagram of a circuit module in accordance with an embodiment of the present invention.

Figure 7 is a block schematic diagram of a memory module in accordance with an embodiment of the present invention.

Figure 8 is a block schematic diagram of an electronic system in accordance with another embodiment the present invention.

Figure 9 is a block schematic diagram of a memory system in accordance with an embodiment of the present invention.

Figure 10 is a block schematic diagram of a computer system in accordance with an embodiment of the present invention.

Description of the Embodiments

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments can be utilized and that process or mechanical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor, as well as other semiconductor support structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process operations may have been utilized to form regions/junctions in the base semiconductor structure. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

The transistors described herein include transistors from bipolar-junction technology (BJT), field effect technology (FET), or complimentary metal-oxide-semiconductor (CMOS) technology. A metal-oxide-semiconductor (MOS) transistor includes a gate, a first node (drain) and a second node (source). Since a MOS transistor is typically a symmetrical device, the true designation of "source" and "drain" is only possible once voltage is impressed on the terminals. The designations of source and drain herein should be interpreted, therefore, in the broadest sense. It should also be noted that a P-channel MOS transistor could alternatively be used for an N-channel MOS transistor and vice versa with the polarity of the associated gate voltages merely being reversed. For example, applying a negative gate voltage in the situation of a P-channel MOS transistor to

activate the transistor and reversing the polarity to apply a positive gate voltage to activate an N-channel transistor if an N-channel MOS transistor is substituted for a P-channel transistor.

Figures 1A-1C illustrate the operations in forming an electrode structure 100 in accordance with the present invention. In Figure 1A, a first layer 102 of conductive material is deposited or formed. The first layer 102 of conductive material can be tungsten, nickel or a semiconductor material. A dielectric layer 104 is formed on the first conductive layer 102. The dielectric layer 104 can be a nitride, such as silicon nitride or a similar dielectric material. The dielectric layer 104 is patterned by standard photolithographic techniques or the like to form at least one opening 106 through the dielectric layer 104 to expose a portion of a surface 108 of the first conductive layer 102. The opening 106 can have a width "W" or a diameter that is significantly larger than a depth "D" to provide a small aspect ratio; however, the invention is not limited to such aspect ratios. A layer 110 of oxide is formed on the dielectric layer 104 and on the surface 108 of the first conductive layer 102. The oxide layer 110 can be a silicon oxide deposited by the thermal reaction of a precursor, such as tetraethyl orthosilicate (TEOS) or the like. The oxide layer 110 can have a thickness between about 50 angstroms and about 200 angstroms. A second layer 112 of conductive material is formed on the oxide layer 110. The second layer 112 of conductive material can be silver, nickel or another metal or conductive material that can diffuse into the oxide layer 110 and bond to the oxide layer 110.

In Figure 1B, the electrode structure 100B is annealed in an inert ambient environment at a selected temperature for a predetermined time period. The inert ambient environment can be nitrogen, argon or some other gas that is non-reactive to the materials forming the electrode structure 100. For an oxide layer 110 of TEOS and a second conductive layer 112 of silver, annealing at about 350° Celsius for about ten minutes provides the proper amount of diffusion or chemisorption of silver molecules into the TEOS to make the oxide layer 110 at least semiconductive so as to not create an electrical barrier between the first and second conductive

layers 102 and 112. The oxide layer 110 is therefore converted into a conductive or at least semiconductive binding layer 110' by the annealing operation. The electrode structure 100B can be annealed at temperatures as low as about 130° Celsius or room temperature; however, the time period to achieve the proper level of chemisorption will be much longer thereby increasing the amount of time overall for the manufacturing process. According to the present invention, the annealing temperature and time period can be adjusted to control the rate and amount of diffusion or chemisorption of molecules of the conductive material or metal from the second layer 112 into the oxide layer 110. The annealing temperature and time period are also selected with consideration of other components and subsequent processing steps so as to not adversely effect or damage other components that have already been formed on a wafer or semiconductor die or that would result in additional processing operations that would increase the cost and time to manufacture a semiconductor chip.

In Figure 1C, the electrode structure can be planarized to form an isolated electrode structure or damascene layer 114 and to form a level or more uniform surface 116 for subsequent processing operations. The planarization of the electrode structure 100C can be accomplished by a chemical/mechanical planarization (CMP) process or the like. In accordance with the present invention, the binding layer 110' is selected to provide sufficient adhesion between the first and second conductive layers 102 and 112 to prevent the forces created by the CMP process from forcing or warping out the damascene layer 114.

In Figures 2A-2D, the process operations are shown to form a programmable memory or metallization cell structure 200 in accordance with an embodiment of the present invention that can be used in a memory system, such as a programmable cell random access memory (PCRAM) device or the like. In Figure 2A, a first conductive layer 202 is formed. The first conductive layer 202 can be a metal, such as tungsten, nickel or the like, or the first conductive layer 202 can be a semiconductor or polysilicon material. A layer 204 of dielectric material is formed on the first conductive layer 202. The dielectric layer 204 can be a nitride, for

example silicon nitride or a similar dielectric. The dielectric layer 204 is selectively patterned by standard photolithographic techniques or similar material removal techniques to form at least one opening 206 in the dielectric layer 204 and to expose a portion of a surface 208 of the first conductive layer 202. The opening 206 can have a depth dimension "D" that is much smaller than a width dimension "W" to define a small aspect ratio of depth to width. The invention, however, is not so limited. A layer 210 of oxide is formed on the dielectric layer 204 and on the exposed surface portion 208 of the first conductive layer 202. The oxide layer 210 can be a silicon dioxide. The oxide layer 210 can have a thickness between about 50 angstroms and about 100 angstroms. A second layer 212 of conductive material is formed on the oxide layer 210 and in the opening 206. The second conductive layer 212 can be a metal, such as silver, nickel, polysilicon or other conductive material that is diffusible into an oxide and exhibits good adhesion to an oxide. The second conductive layer can have a thickness between about 50 angstroms and about 500 angstroms depending upon other parameters or features of the memory cell structure 200.

In Figure 2B, the memory cell structure 200B is annealed at a selected temperature for a predetermined time period in an inert ambient environment, such as nitrogen, argon or some other gas that is non-reactive to the materials forming the cell structure 200. As an example, for an oxide layer 210 of TEOS and a second conductive layer 212 of silver, annealing at about 350° Celsius for about 10 minutes provides the appropriate level of diffusion or chemisorption of silver molecules into the TEOS oxide layer 210 to make the oxide layer 210 at least semiconductive so as to not create an electrical barrier between the first and second conductive layers 202 and 212. The oxide layer 210 becomes a conductive or semiconductive binding layer 210' as a result of the annealing operation and provides stronger adhesion between the first and second conductive layers 202 and 212 as a result of the annealing process for stability of the structure 200 during subsequent manufacturing operations such as CMP. As one of ordinary skill in the art will understand by reading and comprehending this disclosure, the annealing temperature and time can

be adjusted to control the rate and amount of chemisorption of silver or conductive material from the second conductive layer 212 into the oxide layer 210 and to also control the impact on previously formed structures or devices on the wafer or semiconductor chip. Because of the diffusion of conductive material during the annealing process, the resulting conductive binding layer 210' defines an electrical contact or interface between the first and second conductive layers 202 and 212.

In Figure 2C, a layer 214 of chalcogenide glass material is formed on the on the second conductive layer 212 and in the opening 206. The layer 214 of chalcogenide glass material can be germanium selenide (Ge_XSe_{1-X}, where X is the concentration of germanium and 1-X is the concentration of selenide). In one embodiment according to the teachings of the present invention, the concentration ratio of germanium to selenide can be between about 15/85 and about 40/60. A third layer 216 of conductive material is formed on the layer 214. The third conductive layer 216 can be a metal such as silver, nickel or another metal that is diffusible into a chalcogenide material. The layer 214 is doped by annealing the memory cell structure 200C to cause metal or conductive material from the third layer 216 to diffuse into the chalcogenide layer 214 to a selected concentration. The annealing process can be ultra violet annealing or a similar annealing process. The annealing process also improves adhesion between the third conductive layer 216 and the chalcogenide layer 214 resulting in a highly adhesive cell structure 200C that can withstand the forces or pressures applied by subsequent manufacturing operations such as CMP.

In Figure 2D, the cell structure 200D is planarized to form an isolated cell structure 200D or third layer contact or damascene layer 216' and to provide a level or more uniform surface 218 for subsequent processing operations. The cell structure 200D can be planarized by CMP or the like. A fourth layer 220 of conductive material can be formed on the planarized surface 218 and in electrical contact with the third layer contact 216'.

The conductive material or metallization of the second layer 212 formed on the sidewalls 222 of the opening 206 can be minimized by the deposition process

and is substantially diffused into the oxide layer 210 on the sidewalls 222 during the annealing process. In this manner, no isolation or dielectric is required between any residual metallization on the sidewalls 222 and the fourth layer of conductive material 220 that would necessitate additional process steps after the CMP operation and before the fourth layer 220 is formed.

Figures 3A-3E illustrate the operations in forming a programmable memory cell 300 in accordance with another embodiment of the present invention that forms a reentrant profile to prevent conductive material from forming on the sidewalls of the opening in the dielectric layer. In Figure 3A, a first conductive layer 302 is formed. The first conductive layer 302 can be a metal such as tungsten, nickel, or the like, or a semiconductor material or polysilicon. A first dielectric layer 304 having one etch rate is formed on the first conductive layer 302 and a second dielectric layer 306 having a second etch rate is formed on the first dielectric layer 304. In accordance with the present invention, the etch rate of the first dielectric layer 304 is faster than the etch rate of the second dielectric layer 306. Accordingly, in Figure 2B, when the first and second dielectric layers 304 and 306 are selectively patterned to form an opening 308, the opening has a reentrant profile with sidewalls 310 that angle back as the opening 308 extends down to expose the first conductive layer 302. A layer 312 of oxide is formed on the second dielectric layer 306 and on an exposed surface portion 314 of the first conductive layer 302 in the opening 308. The oxide layer 312 can be a silicon oxide. A second layer 316 of conductive material is formed on the oxide layer 312. The second conductive layer 316 can be silver, nickel or another conductive material or metal that is diffusible into an oxide. Because of the reentrant profile of the opening 308, the second conductive layer 316 and oxide layer 312 cannot form on the sidewalls 310 of the opening 308.

In Figure 3C, the cell structure 300C is annealed at a selected temperature for a predetermined time period to cause metallization or conductive material from the second conductive layer 316 to diffuse into the oxide layer 312 to form a conductive binding layer 312'. The conductive binding layer 312' provides electrical contact and adhesion between the first and second conductive layers 302 and 316

during subsequent processing operations such as CMP. As previously discussed, the annealing temperature and time can be adjusted to control the amount of chemisorption of metal molecules into the oxide layer 312 and to control the impact on other components or devices already formed on the wafer or semiconductor chip.

In Figure 3D, a layer 318 of chalcogenide glass material is formed on the on the second conductive layer 316 and in the opening 308. The layer 318 of chalcogenide glass material can be germanium selenide (Ge_XSe_{1-X}, where X is the concentration of germanium and 1-X is the concentration of selenide). As previously discussed, according to the teachings of the present invention, the concentration ratio of germanium to selenide can be between about 15/85 and about 40/60. A third layer 320 of conductive material is formed on the layer 318. The third conductive layer 318 can be a metal such as silver, nickel or another metal that is diffusible into a chalcogenide material. The layer 318 is doped by annealing the memory cell structure 300D to cause metal or conductive material from the third layer 320 to diffuse into the chalcogenide layer 318 to bond the two layers together and provide better adhesion.

In Figure 3E, the cell structure 300E is planarized to form an isolated cell structure 300E including an isolated third layer contact or electrode 320'. The planarization also provides a level, more uniform surface 322 for subsequent processing operations. The cell structure 300E can be planarized by CMP or the like. A fourth layer 324 of conductive material can be formed on the planarized surface 322 and in electrical contact with the third layer electrode or contact 320'.

In operation, the programmable memory cell 200 or 300 or programmable metallization cell can be programmed by applying a potential or voltage across the first layer or electrode 302 and the third layer electrode 320' that has a sufficient voltage level to cause a dendrite 326 or conductive filament to be formed between the electrode 320' and the second conductive layer 316 which is electrically connected to the first layer electrode 302 by the conductive binding layer 312'. Because the chalcogenide layer 322 is doped with a metal or conductive material such as silver, the voltage causes the dendrite 326 (226 in Figure 2D) to be formed

to short circuit the two electrodes 320' and 302. The resistance across a cell 300 that has been biased by applying sufficient voltage to form the dendrite 326 is about 10,000 ohms. The resistance of a cell 300 that has not been biased and is in an open condition is about 10 megohms. Accordingly, a programmed cell 300 to which a voltage has been applied to form the dendrite 326 can represent a logic 1 and an unprogrammed or open cell 300 can represent a logic 0. To erase a programmed cell 300, a reverse polarity voltage can be applied to the electrodes 320' and 302 of the cell 300 to cause sufficient current to flow through the cell 300 to return the cell 300 to a high resistance state by destruction of the dendrite 326 or conductive element.

Figure 4 is a schematic diagram of a memory device or system 400 in accordance with the present invention. The memory system 400 includes a plurality of memory elements 402 that can be arranged in rows and columns. Each memory element 402 can include a transistor 404. Each transistor 404 includes a gate electrode 406 coupled to an address line 408 for controlling the operation of the memory element 402, and each transistor 404 includes a first source/drain electrode 410 coupled to a data line 412 and a second source/drain electrode 414 coupled to a programmable memory cell 416 according to the teachings of the present invention, e.g. similar to the memory cells 200D (Figure 2D) and 300E (Figure 3E).

With reference to Figure 5, a semiconductor die 510 can be produced from a silicon wafer 500 that can contain a memory system similar to system 400 or an electronic system including the novel electrode structure 100C (Figure 1E) or memory cells 200D (Figure 2D) or 300E (Figure 3E) in accordance with the present invention. A die 510 is an individual pattern, typically rectangular, on a substrate that contains circuitry to perform a specific function. A semiconductor wafer 500 will typically contain a repeated pattern of such dies 510 containing the same functionality. Die 510 can further contain additional circuitry to extend to such complex devices as a monolithic processor with multiple functionality. Die 510 is typically packaged in a protective casing (not shown) with leads extending

therefrom (not shown) providing access to the circuitry of the die 510 for unilateral or bilateral communication and control.

As shown in Figure 6, two or more dies 510, including at least one electronic system or memory system 400 that incorporates the novel electrode structure 100C or memory cells 200D or 300E in accordance with the present invention, can be combined, with or without a protective casing, into a circuit module 600 to enhance or extend the functionality of an individual die 510. Circuit module 600 can be a combination of dies 510 representing a variety of functions, or a combination of dies 510 containing the same functionality. Some examples of a circuit module 600 include memory modules, device drivers, power modules, communication modems, processor modules and application-specific modules and can include multi-layer, multi-chip modules. Circuit module 600 can be a sub-component of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft and others. Circuit module 600 will have a variety of leads 610 extending therefrom providing unilateral or bilateral communication and control.

Figure 7 shows one embodiment of a circuit module as a memory module 700 containing circuitry for the memory system 400 including the electrode structure 100C or memory cell structures 200D or 300E of the present invention. Memory module 700 generally depicts a Single In-line Memory Module (SIMM) or Dual In-line Memory Module (DIMM). A SIMM or DIMM can generally be a printed circuit board (PCB) or other support containing a series of memory devices. While a SIMM will have a single in-line set of contacts or leads, a DIMM will have a set of leads on each side of the support with each set representing separate I/O signals. Memory module 700 contains multiple memory devices 710 contained on support 715, the number depending upon the desired bus width and the desire for parity. Memory module 700 can contain memory devices 710 on both sides of support 715. Memory module 700 accepts a command signal from an external controller (not shown) on a command link 720 and provides for data input and data output on data links 730. The command link 720 and data links 730 are connected

to leads 740 extending from the support 715. Leads 740 are shown for conceptual purposes and are not limited to the positions shown in Figure 7.

Figure 8 shows an electronic system 800 containing one or more circuit modules 600 as described above containing the novel memory system 400 and electrode structure 100C or memory cells 200D or 300E of the present invention. Electronic system 800 generally contains a user interface 810. User interface 810 provides a user of the electronic system 800 with some form of control or observation of the results of the electronic system 800. Some examples of user interface 810 include the keyboard, pointing device, monitor and printer of a personal computer; the tuning dial, display and speakers of a radio; the ignition switch and gas pedal of an automobile; and the card reader, keypad, display and currency dispenser of an automated teller machine. User interface 810 can further describe access ports provided to electronic system 800. Access ports are used to connect an electronic system to the more tangible user interface components previously exemplified. One or more of the circuit modules 600 can be a processor providing some form of manipulation, control or direction of inputs from or outputs to user interface 810, or of other information either preprogrammed into, or otherwise provided to, electronic system 800. As will be apparent from the lists of examples previously given, electronic system 800 will often contain certain mechanical components (not shown) in addition to the circuit modules 600 and user interface 810. It will be appreciated that the one or more circuit modules 600 in electronic system 800 can be replaced by a single integrated circuit. Furthermore, electronic system 800 can be a sub-component of a larger electronic system.

Figure 9 shows one embodiment of an electronic system as memory system 900. Memory system 900 contains one or more memory modules 700 as described above including the memory system 400 and electrode structure 100C or memory cells 200D and 300E in accordance with the present invention and a memory controller 910. Memory controller 910 provides and controls a bidirectional interface between memory system 900 and an external system bus 920. Memory system 900 accepts a command signal from the external bus 920 and relays it to the

one or more memory modules 700 on a command link 930. Memory system 900 provides for data input and data output between the one or more memory modules 700 and external system bus 920 on data links 940.

Figure 10 shows a further embodiment of an electronic system as a computer system 1000. Computer system 1000 contains a processor 1010 and a memory system 900 housed in a computer unit 1005. Computer system 1000 is but one example of an electronic system containing another electronic system, i.e. memory system 900, as a sub-component, including the memory system 400 and electrode structure 100C or memory cells 200D and 300E in accordance with the present invention. Computer system 1000 optionally contains user interface components. Depicted in Figure 10 are a keyboard 1020, a pointing device 1030, a monitor 1040, a printer 1050 and a bulk storage device 1060. It will be appreciated that other components are often associated with computer system 1000 such as modems, device driver cards, additional storage devices, etc. It will further be appreciated that the processor 1010 and memory system 900 of computer system 1000 can be incorporated on a single integrated circuit. Such single package processing units reduce the communication time between the processor 1010 and the memory system 900.

Conclusion

The present invention thus provides an electrode structure and memory cell structure and method of fabrication that provides substantially improved adhesion between two layers of conductive material during subsequent processing operations, such as a CMP operation. The electrode structure and memory cell structure of the present invention also can provide a conductive interface between the two conductive layers that is not an electrical barrier and can provide a doped glass layer that can be programmed to store data. The present invention also provides a method of fabricating an electrode structure or memory cell structure that does not adversely effect subsequent processing operations or require additional processing operations

and the process can be controlled to avoid damage to other components that may already have been formed on the same wafer or substrate.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.